IBIS QUALITY SPECIFICATION
Revision 1.1at (draft)
20 July 2009

Purpose

This document is a specification covering a methodology to enhance the quality of electronic component model files produced in conformance with the ANSI/EIA-656-A I/O Buffer Information Specification (IBIS). More information on the IBIS specification can be found on the IBIS web page:

http://www.eigroup.org/ibis/default.htm

The purpose of the IBIS Specification is to provide a standard for model data exchange and thus to enhance the value of modeling and simulation.

The purpose of this IBIS Quality Specification is to provide a methodology for validating model data against the IBIS Specification and a means of objective measures of correlating model simulation results with measurements or other model simulations. By providing standards for validating, correlating, and replicating simulation results we seek to enhance the value of modeling and simulation.

Neither standard is a means, by itself, for guaranteeing quality. The quality of models and simulations are largely the result of market forces. Standards serve to enhance the exchange of data.

This IBIS Quality Specification is intended to supplement existing support mechanisms for producers of IBIS files. Email reflectors for IBIS community support are open to the public. Details on the email reflectors and the model review service offered by the IBIS Open Forum are described at the web URL given above.

Revision History

1.0a	31-mar-2004	Bob Haller	Initial version
1.0b	04-jan-2005	Mike LaBonte	Review update
1.0c	15-feb-2005	Mike LaBonte	Review update
1.0d	08-mar-2005	Mike LaBonte	Review update
1.0e	05-apr-2005	Bob Haller	Review update
1.0f	12-apr-2005	Mike LaBonte	Review update
1.0g	02-aug-2005	Mike LaBonte	Review update
1.1a	14-aug-2006	Moshiul Haque	Modified section 1, 2, 3, 4 and 5 with the new IQ numbering scheme Added "Receiver Threshold" as an optional requirement in section 4
1.1b	31-oct-2006	Mike LaBonte	Convert to MSWord format.
1.1c	27-nov-2006	Mike LaBonte	Review update
1.1d	12-dec-2006	Mike LaBonte	Review update
1.1e	09-jan-2007	Mike LaBonte	Formatting. More formatting work needed beginning at 4.3.10.
1.1f	23-jan-2007	Mike LaBonte	Change “exemption” to “exception”.
1.1g	6-feb-2007	Mike LaBonte	Changes to section 2.1.
1.1h	13-feb-2007	Bob Ross/Moshiul Haque	Added detail explanation regarding “X” in section 2.1
1.1i	20-feb-2007	Kim Helliwell/Mike LaBonte	Changes to 4.1.3 and 4.1.4. Restore IBISCHK NOTES from 5-jul-2005 version.
1.1j	20-feb-2007	Mike LaBonte	Changes from 20-feb-2007 meeting.
1.1k	27-feb-2007	Mike LaBonte	Extended Purpose to discuss IBIS support.
1.1l	26-mar-2007	Mike LaBonte	Replaced 4.1.4 and 4.3 with material from David Banas. Change 3.1.3 to IQ1.
1.1m	30-mar-2007	Mike LaBonte	Change limits in 3.1.2 and add ibischk notes.
1.1n	16-apr-2007	Kim Helliwell, Mike LaBonte	Changes to 3.1.2, 3.1.3, 3.1.4 (deleted), and 3.2.1.
1.1o	24-apr-2007	Kim Helliwell, Mike LaBonte	Suggest Terminator model in 3.2.1. Merge 3.2.5 into 3.2.4. Deleted 3.1.3, 3.2.2, 3.2.3, 3.2.5.
1.1p	3-May-2007	Mike LaBonte	Updated 3.2.5 and 3.3.2. Deleted 3.3.1.

1.1q	21-May-2007	Roy Leventhal, Mike LaBonte	Fixed RLC requirement in 3.2.5. New text for 3.3.2. Deleted 3.3.3. Changed 3.3.4 to require a comment for exceptions.
1.1r	18-Jun-2007	Moshiul Haque, Mike LaBonte	3.3.4 becomes LEVEL 2. Deleted 3.4.1. Inserted 3.4.3 and 3.4.4.
1.1s	19-Jun-2007	Mike LaBonte	Small changes to 3.4.3 and 3.4.4.
1.1t	10-Jul-2007	Mike LaBonte	Deleted 3.4.2. Renumbered so that [Model Selector] checks are in new section 4, all subsequent sections renumbered.
1.1u	30-Jul-2007	Bob Ross, Roy Leventhal, Mike LaBonte	Revisions to 5.1.1, 5.1.7, and 5.1.8. Deleted 5.1.2 and 5.1.9 through 5.1.12.
1.1v	14-Aug-2007	Mike LaBonte, Roy Leventhal	Revisions to 5.1.7, 5.1.8, 5.2, and 5.2.2. Deleted 5.2.1, 5.2.3, and 5.2.4.
1.1x	11-Sep-2007	Mike LaBonte	Updated 5.2.2, 5.2.5, 5.2.6, and 5.2.22. Deleted 5.2.7 and 5.2.8. Further edits to 5.2.2 from Roy Leventhal.
1.1y	11-Dec-2007	Roy Leventhal, Mike LaBonte	5.2.2, 5.2.18. 5.2.3, 5.2.4, 5.2.7, 5.2.8, 5.3.4 updated, 5.2.17, 5.3.3 marked for deletion. Fixed swapped M & S in 5.3.17.
1.1z	15-Jan-2008	Mike LaBonte	5.2.16, 5.2.18 updated. Notes removed from 5.2.21 & 5.2.13.
1.1aa	22-Jan-2008	Mike LaBonte	Change all “datasheet” to “data sheet”. Change some check titles to “present and matches data sheet”. Change 5.1.4 from “correct” to “reasonable”. Merged “present” checks and “correct” checks for [Receiver Thresholds]. Minor editorial changes.
1.1ab	29-Jan-2008	Mike LaBonte	Wording changes in 5.2.18, 5.2.20, 5.2.24.
1.1ac	20-Feb-2008	Mike LaBonte	Cleanup of 5.3, 5.3.1 marked for deletion, 5.3.2 clarified.
1.1ad	17-Mar-2008	Mike LaBonte	5.2.5 clarified. 5.3.4, 5.3.5, 5.3.6, and 5.3.7 updated.
1.1ae	29-Apr-2008	Mike LaBonte	Add G designator.
1.1af	15-July-2008	Mike LaBonte	5.2.9 clarified. 5.2.10, 5.2.11, 5.2.12 marked for deletion.
1.1ag	16-July-2008	Mike LaBonte	Update 5.2.16. Add 5.2.17. Change 5.3.2-10 checks to LEVEL 2. Update 5.3.8-10. Add 5.3.11.

1.1ah	26-Aug-2008	Mike LaBonte	Clarifications to 5.2.12-15.
1.1ai	30-Sep-2008	Mike LaBonte	5.3.13 and 5.4.5 updated. 5.3.17, 5.4.1, 5.4.3, and 5.4.4 marked for deletion.
1.1aj	18-Nov-2008	Mike LaBonte	5.5.1, 5.5.3, 5.5.5 and 5.5.9 marked for deletion. 5.5.7 and 5.5.8 clarified.
1.1ak	6-Jan-2009	Mike LaBonte	Deleted items marked for deletion. Checks are now renumbered.
1.1al, 1.1am	17-Mar-2009	Mike LaBonte	5.3.10, 5.3.11, 5.4.1 through 5.4.4 updated. 5.6, 5.6.1, and 5.6.2 added from 6.1 and 6.3..1 updated. 6.2 and 6.3 deleted. Outline numbering format repaired. NOTE: Changes for 1.1al and 1.1am are listed here.
1.1an	07-Apr-2009	Mike LaBonte, Moshiul Haque	6.1 text moved to 5.1.2. Section 7 mostly rewritten. 1.2.2 and 1.2.3 updated. LVDS clarification added to 5.4.1. All of section 6 is now empty, marked for deletion.
1.1ao	21-Apr-2009	Mike LaBonte	Completely deleted section 6. Deleted section 8, moved documentation requirements to section 1. Note: “Correlation” was section 7 and is now section 6.
1.1ap	15-May-2009	Mike LaBonte	Clarified placeholder status of the IQ4 level. Replaced text of 1.4. Deleted 5.5.3 ([Ramp] dV vs. supply voltage), so that checks 5.5.4 and 5.5.5 are now 5.5.3 and 5.5.4. What is now 5.5.3 was a V-T table endpoints vs. [Ramp] dV check, now replaced with a new I-V table vs. [Ramp] dV check. Reference to 5.5.7 replaced with method description text in what is now 5.5.4.
1.1aq	19-May-2009	Mike LaBonte	Updated 1.1.5 and 1.4. Some editorial cleanup.
1.1ar	02-Jun-2009	Mike LaBonte	Editorial cleanup.
1.1as	09-Jun-2009	Mike LaBonte	Editorial cleanup and clarifications in section 1.
1.1at	20-Jul-2009	Mike LaBonte	Font cleanup. Editorial changes in 3.1.2, 3.2.1, 5.3, 5.3.8, and 5.3.9.

Table of Contents

1. IBIS Quality Designator

The quality of an IBIS file can be determined by checking its data for correctness, and by correlating the data to a reference. Correctness is defined as conforming to a designated version of the IBIS Specification and the component data sheet. A number of individual checks are performed, and the overall file quality is represented with a designator such as "IQ3S", for example, which would indicate that data for basic simulation and timing analysis have been checked, and the IBIS model has been correlated to a reference simulation. The summary IBIS Quality designator is embedded in the IBIS file as a comment or in the [Notes] section

1.1. IBIS Quality Level Definitions

The quality level is defined as a combination of correctness checks and correlation checks. The correctness level is a number, and other special designations such as correlation are shown as appended letters. Some examples:

- **IQ0** - No IQ checking at all.
- **IQ1** - Passes IBISCHK without errors or unexplained warnings.
- **IQ2** - IQ1 + data for basic simulation checked.
- **IQ3** - IQ2 + data for timing analysis checked
- **IQ4** - IQ3 + data for power analysis checked
- **IQ3M** - IQ3 + correlated against hardware measurements
- **IQ3MS** - IQ3 + correlated against measurements and simulation
- **IQ3GS** – IQ3 + golden waveforms + correlated against simulation
- **IQ4X** - IQ4, but exception(s) to check(s) commented in file

The 5 recognized levels of correctness checks and 3 levels of correlation checks are discussed below. Details of the referenced checks and correlation tests are given in sections 2 through 7.

1.1.1. IQ0 – Not Checked

An IQ0 file has not been checked, or at least the checking has not been documented. This is a placeholder level useful for showing which files are queued for checking. Tools that create IBIS files should put IQ0 comments in the files.

1.1.2. IQ1 – Passes IBISCHK

An IQ1 file has been checked with the latest IBISCHK parser at the time of checking.

- The version of IBISCHK used must be documented in the Quality Summary.
- IBISCHK must report 0 Errors
- All IBISCHK warnings must be explained if they cannot be eliminated. Ideally, there should be no warnings, but it is recognized that some warnings cannot be eliminated. It is not necessary to flag exceptions with an IQ1X designation in this case.

1.1.3. IQ2 – Suitable for Waveform Simulation

An IQ2 file can be simulated with reasonable assurance that the buffer signal waveforms are correct. It does not necessarily have accurate per-pin or coupled package modeling, may not have information needed to check timing, and may not have information to help measure power currents. IQ2 includes all items in IQ1, plus the following checks:

1.1.4. IQ3 – Suitable for Timing Analysis

An IQ3 file is suitable for signal timing analysis. Package modeling at the pin level is present and accurate, and special keywords for measuring timing are present and correct. Coupled package modeling is not required. IQ3 includes all items in IQ2, plus the following checks:

1.1.5. IQ4 – Suitable for Power Analysis

An IQ4 file is suitable for power analysis. The power and ground currents associated with groups of buffers are accurately modeled. This is distinct from the signal analysis capabilities addressed by IQ2 and IQ3. This is a placeholder, since no IQ level 4 checks are currently defined. These checks will be defined in a future version of the IBIS Quality Specification. Currently no IBIS file can have an IQ4 level.

1.2. Special Designators

The following special designator letters can be appended to the IQ level to convey additional important information.

1.2.1. Designator "G" – Contains Golden Waveforms

Special designator “G” indicates that the file contains golden waveforms, the [Test Data] and [Test Load] keywords defined in IBIS 4.0. Users can compare simulations of IBIS buffer models with the same test loads against the corresponding golden waveforms. Golden waveforms must be produced from source simulations or measurements, not from simulations of IBIS models. The set of [Test Load] fixtures used must include at least one with a transmission line. The “G” designator may be used with IBIS files containing golden waveforms for only a subset of buffer models, as determined by sound engineering judgment.

1.2.2. Designator "M" – Measurement Correlated

Special designator "M" indicates that measurement correlation has been performed and the results are deemed satisfactory. The “M” designator may be used with IBIS files containing golden waveforms for only a subset of buffer models, as determined by sound engineering judgment. More on correlation can be found in section 6.

1.2.3. Designator "S" – Simulation Correlated

Special designator "S" indicates that simulation correlation has been performed and the results are deemed satisfactory. The “S” designator may be used with IBIS files containing golden waveforms for only a subset of buffer models, as determined by sound engineering judgment. More on correlation can be found in section 6.

1.2.4. Designator "X" - Exceptions

Special designator "X" refers to exception from correctness or correlation. Exceptions should be used to declare that the file is suitable for the purpose indicated by the IQ level even though one or more checks are not passed by strict standards. The reason for the exception must be documented in the {Notes] section. Before using an IBIS file with the X designator in its IQ level, the model user should open the file and look for comments explaining exceptions.

1.3. OPTIONAL Checks

A limited number of IQ checks have {OPTIONAL} in the title instead of a {LEVEL n} designator. While considered good practice, these checks are not required to achieve any IQ level. This is generally used where data is not commonly available in suitable form for the IBIS representation.

1.4. IBIS Quality summary

The summary IQ score for an IBIS file is determined as follows:

- The summary IQ level number is the highest for which all checks of that level are passed.
- “M”, “S”, and/or “G” designators are appended to the summary IQ score if a reasonable set of models have been measurement and/or simulation correlated, or if the file contains golden waveforms, respectively.
- “X” is appended to the summary IQ score if any check in the file can not be passed without exception.
- OPTIONAL checks have no effect on the summary IQ score.

The summary IQ score must be posted in the IBIS file. This should appear in the [Notes] section, but comment lines are acceptable. Any exceptions must also be explained in the IBIS file. An example IQ summary in an IBIS file might look like this:

```
|IQ Score: IQ3SX
|IQ Exception: Correlation not performed for untimed low speed signals
```

The pass/fail status of individual IQ checks may be posted in the file as comments, or contained in a separate document such as an IBIS file quality report. The latter is preferred, especially if the report also contains details such as waveforms, correlation metrics, and reviewer’s notes. For each check the ID number and IQ level of the check should be stated, along with the name of any [Component] or [Mode] to which it applies, as well as the pass/fail status.

2. General Header Section Requirements

Requirements for the header section of the IBIS file, from the beginning of the file to the line before the first [Component] keyword.

2.1. {LEVEL 1} IBIS file passes IBISCHK

IBIS models are expected to pass the checks performed by the IBISCHK program before they are released to the public. Passing IBISCHK insures that the file will attain at least an IQ1 level designation. The IBISCHK program is found at http://www.eigroup.org/ibis/tools.htm.

A best practice is to insert the full output from the IBISCHK program into the IBIS file as comments, with explanation for any warnings annotated within. When doing this it is important to insure that the added comments do not cause new "line too long" IBISCHK warnings.

In general it is best to use the latest available version of the IBISCHK program, as the latest version may include new tests and fixes for bugs found in the older versions. The IBISCHK program used must, at a minimum, be able to accommodate the [IBIS Ver] of the IBIS file at hand. The [IBIS Ver] used in the IBIS file is set by the model maker based on the set of IBIS keywords required to completely and correctly represent the behavior of the part. The [IBIS Ver] value can be set to at least 3.2 because this version is supported by a wide variety of EDA tools. It should not be necessary to avoid IBIS 3.2 features to achieve compatibility with IBIS tools. Also, version 3.2 includes IBIS keywords that are needed to correctly describe many I/O buffers in use today.

Some IBISCHK warnings may be permissible due to special circumstances regarding the model, but they must be identified in the IBIS file itself in the [Notes] section of the file. The warnings, along with the reason why they should be considered acceptable must be identified. Also the IQ level designator must include "X" for exceptions due to warnings.

The X (exception) designation is used to document all exception cases that might be important to some user. These would mostly apply to Warning messages where the model provider gives further information. The X designation may also apply to cases where the extracted or specification information has been changed, and its impact. Finally it can also be used for any unusual situation in the parser, where the model information is correct, but the parser still issues Warning or Caution messages. The main point is that the model provider has purposely issued the model with some deviation, and the user needs to know about its details to understand the issues that might arise in using the model.

For some minor deviations including where model data is changed to eliminate Warning messages, the X designation might not be needed. For example, the X would normally not be used for I-V table regions where some non-monotonic data due to measurement noise or spurious data is removed. The changed data has minimal impact on model simulations and helps increase model portability.

Occasionally a problem exists with IBISCHK rather than with the model. While the IBISCHK problem may be fixed in the future, the existing model could be tagged with X and contain a description of its issues and how this may impact how the IBIS model is used. In the event an error is generated due to a specific bug in the IBISCHK, intentional deviation in the model may be permitted to suppress the error in the model provided such deviations are properly documented in the [Notes] section with "X" tagged in the quality designation. This suppression of error is a unique case and should have minimal impact on the accuracy of the model.

A Level 1 Model must NOT produce ANY errors when run through IBISCHK.

Summary:

- The goal is zero errors and zero warnings.
- In some cases zero warnings are not possible.
- Add the "X" designator to the IQ level if there are warnings.
- Document known cases of acceptable warnings.
- Document the version of IBISCHK used.
- A list of past File Rev/Dates and the reason for each model change.

3. Component Section

Checks for the [Component] section may be waived for IBIS files for programmable parts such as FPGAs, if the file is generic in nature, and does not represent a final, programmed part. In generic IBIS files the [Pin] section typically contains one entry for each [Model], but it does not correspond to any actual device pin map.

3.1. Component Package Requirements

Requirements for the [Package] and [Package Model] sections:

3.1.1. {LEVEL 2} [Package] must have typ/min/max values

The IBIS specification requires Typ values in the [Package] keywords, and allows Min and Max values to be NA if not available. To achieve IQ level 2 an IBIS file must have Typ, Min and Max values in the [Package] keywords. A reflection analysis based only on Typ package parasitics is likely to be optimistic. Min and Max values are required to insure that peak distortion levels are predicted.

3.1.2. {LEVEL 2} [Package] Parasitics must be reasonable

Reasonable values for signal pins are: L < 100nH, C < 100pF, R < 10 ohm. Min must be less than typ and typ less than max.

The IBISCHK program detects typographical errors such as omitting the scaling factor following a number value, by checking against higher limits: L < 1000nH, C < 1000pF, R < 50 ohm. An R_pkg value of 1000 would easily fail this test, for example. This IQ check, with its lower limits, will detect other errors such as extra digits or measurement error.

The min and max values of these parasitics should represent the range spanned by the actual pin parasitics for signal pins. The typical values should fall between the min and max values; typically it is the average of the signal pin parasitics, but it need not be. Methods and assumptions used, such as whether power and ground pins are included in the determination of the [Package] parasitics, should be documented as comments.

3.2. Component Pin Requirements

Requirements for the [Pin] section:

3.2.1. {LEVEL 2} [Pin] section complete

All pins must be defined for a component. In addition to signal pins:

- No Connects must be represented with model name NC.
- Power pins must be indicated model name POWER.
- Ground pins must be indicated model name GND.
- The variety of [Model]s assigned to pins matches the variety of buffer characteristics described in the datasheet, and each pin has the correct [Model] or [Model Selector] assigned to it.
- Special Pins (e.g. analog) are to be represented in the [Pin] section, even if they are marked NC. Explanatory comments are recommended for these. A common practice is to represent analog pins with Terminator models, so that waveforms of crosstalk received at the pins can be viewed in EDA tools.

For IBIS buffer [Model] libraries, it is recommended that one pin be used for every model and that the pin name be the same as the model name.

3.2.2. {LEVEL 3} [Pin] RLC parasitics are present and reasonable

For a LEVEL 2 model, pin parasitics are optional, but they are mandatory for a LEVEL 3 model (that is, a model suitable for timing). To pass this check the RLC values must be present for all signal pins in the [Pin] section, or [Package Model] must be present. Pin parasitics should either be measured or extracted using a 2D or 3D solver. Reasonable signal pin parasitics will result in impedance and delay characteristics that fall in the ranges:

TD = SQRT(LC) < 300ps

Z0 = SQRT(L/C) < 100ohm

Note that IQ check 3.1.2. also requires that each [Pin] RLC value falls within the min/max range as given by the [Package] keyword. The [Package] keyword can be adjusted to accommodate.

3.3. Component Diff Pin Requirements

Requirements for the optional [Diff Pin] section:

3.3.1. {LEVEL 3} [Diff Pin] Vdiff and Tdelay_* complete and reasonable

For input and I/O pins Vdiff must be defined, non-zero and positive. For output and I/O pins Tdelay_typ, Tdelay_min, and Tdelay_max data can be zero, but must be defined. Both Vdiff and Tdelay_* are measured relative to the die pads and must not include additional package delays and offsets. Output pins should have NA for Vdiff. For input pins Tdelay_typ, Tdelay_min, and Tdelay_max must be NA.

3.3.2. {LEVEL 2} [Diff Pin] referenced pin models matched

It is expected that both pins of a differential pair will use the same [Model]. If the buffer models referenced by the two physical pins of a [Diff Pin] entry are not the same [Model] name, a comment or [Notes] entry must be present to explain why.

4. Model Selector Section

4.1. {LEVEL 2} [Model Selector] entries have reasonable descriptions

Each line the [Model Selector] keyword must have two fields. The first field lists the referenced [Model] name and second field contains a short description of the model shown in first field. The purpose of the description is to aid the user of the EDA tool in making intelligent buffer model selections. It can be used by the EDA tool in a user interface dialog box as the basis of an interactive buffer selection mechanism. An example of usage of model selector with an appropriate description might be a programmable buffer in DDR3, where the description may include the impedance of the driver and the applicable maximum frequency of the model (800 Mbps, 34 Ohm Data I/O with no ODT). It is recommended to have a specific description in the [Notes] section about the existence of [Model Selector] in an IBIS file with a short explanation of why it was used, possibly with references to the data sheet for further explanation.

4.2. {LEVEL 2} Default [Model Selector] entries are consistent

The first entry under each [Model Selector] keyword is the default entry. They will be the models used by EDA tools if the user makes no specific choice. The set of default entries should be consistent, describing a state that may likely exist on the part, considering dependencies between them. For example, if the [Model Selector] entries describe controlled output impedances for a part on which all buffers are set to the same impedance, then the default entries for all [Model Selector]s would have the same impedance. We must not have one [Model Selector] defaulting to 35 ohms and another to 50 ohms in that case. Furthermore, the most frequently used setting of a [Model Selector] is the preferred default, if that can be determined.

5. Model Section

5.1. Model General Requirements

5.1.1. {LEVEL 2} [Model] parameters have correct typ/min/max order

For [Model] parameters, Min corresponds to the conditions for weak/slow buffers, Max corresponds to conditions for strong/fast buffers. These conditions are controlled by buffer selections for process, temperature and voltage conditions.

Normally all keywords and subparameters scoped by the [Model] keyword with typ/min/max data has three columns corresponding to typical, weak/slow, and strong/fast, in order. The major exception is C_comp (including C_comp_*), which uses the numerically lowest value for Min, and numerically highest for Max. The highest [Temperature] value may fall into the Min column or the Max column, depending on technology. For CMOS technology the highest [Temperature] usually results in slow/weak operation, and would appear in the Min column.

5.1.2. {LEVEL 2} [Model] C_comp is reasonable

When present in the model as an alternative to the overall C_comp value, C_comp_pullup, C_comp_pulldown, C_comp_power_clamp, and C_comp_ground_clamp, or any combination thereof chosen to represent the die capacitance of the buffer, must sum to the original C_comp

value. In other words, specifying the die capacitance in this more specific way should not change its overall value.

Note that a model may contain a combination of C_comp_* parameters that appear inconsistent with the buffer type. For instance, an open-drain model might include the C_comp_pullup parameter. This is because a pullup structure, for instance, may exist in the silicon and simply not be used for a particular I/O type. However, its parasitic capacitance will still be present at the node.

All general notes regarding choice of capacitance to report, given that die capacitance is frequency/voltage dependent, that apply to the C_comp parameter apply here as well.

As is the case with C_comp, the C_comp_* parameters must be positive. Also, cases in which the total of the C_comp_* values is greater than 20pF should be explained in the [Notes] section, as is suggested for C_comp.

```
The values for C_comp must be checked for plausibility.  Sometimes a compromise
must be reached because C_comp in driving mode and C_comp in non-driving mode
can be different. However, IBIS allows us to specify only a single value for
total C_comp.

The process of determining the appropriate C_comp depends on the type of
systems in which the device is being used. For example, topology and datarate
can affect the choice of C_comp. For low frequency point-to-point terminated
systems, the effect of C_comp on signal integrity is typically less than high
frequency systems with complex topologies. The model maker is encouraged to
make necessary adjustments in C_comp that give the best correlation with spice
simulation or with measurement data.

One approach is to include both driving mode and non-driving mode C_comp
values, with one commented out. An alternative is to calculate the average
values. A suggested practice is to offer all of the above using comment lines
to allow selection by the user:

       C_comp   3.0p 2.9p 3.1p   | C_comp_non-driving
      |C_comp   4.0p 3.9p 4.1p   | C_comp_driving
      |C_comp   3.5p 3.4p 3.6p   | (C_comp_non-driving + C_comp_driving) / 2
```

The set of values is not restricted to those shown above. C_comp might also be computed for other combinations of voltage and frequency.

5.1.3. {LEVEL 2} [Temperature Range] is reasonable

To pass this check the [Temperature Range] keyword must be present. The keyword needs some explanation because “minimum (min)” corresponds to a slow, weak driver and “maximum (max)” corresponds to a fast, strong driver. Slow and fast, in relation to temperature, depends on the process technology being described.

Normally, CMOS has the relationship:

```
Temp(Min) > Temp(Max)
```

While Bipolar normally has:

```
Temp(Min) < Temp(Max)
```

Mixed and temperature-compensated technologies could go either way.

The [Temperature Range] specified should normally match the temperatures at which the model was extracted. This is the chip die temperature, NOT the ambient temperature. The temperature

being specified is usually higher than ambient temperature because the IC and parts around it in the measurement setup (or simulation) dissipate power. If the [Temperature Range] might not accurately represent chip die temperature, this should be documented in a comment.

The reasons for differences between [Temperature Range] keyword and any model extraction temperature ranges should be documented as an exception, or comment.

The [Temperature Range] should not exceed the safe operating temperature range as given on the data sheet.

5.1.4. {LEVEL 2} [Voltage Range] or [* Reference] is reasonable

[Voltage Range] is the operating supply voltage for a [Model]. It is required unless ALL FOUR of the other voltage reference keywords are supplied. When [Voltage Range] is used alone, the other keywords default to:

[Pullup Reference] = [Voltage Range] value

[Pulldown Reference] = 0V

[POWER Clamp Reference] = [Voltage Range] value

[GND Clamp Reference] = 0V

Regardless of whether [Voltage Range] or [* Reference] is used, the values must be reasonable and must represent the actual conditions of IBIS model extraction. The typ, min and max values of the chosen voltages should normally follow the relationship:

min < typ < max

The min and max voltages must fall within the maximum operating conditions specified by the data sheet, but are not required to span the full range. Model users will be looking for min and max voltages that will reflect the range of supply voltages for their design, which will usually not stray more than 10% from the nominal voltage. If a buffer can be operated at more than one nominal voltage, a separate [Model] should be created for each nominal voltage, with reasonable min and max values for each typ voltage. In this case [Model Selector] would be used to allow the user to choose the nominal voltage used for the application.

There should be consistency among models of the same nominal voltage. For example, all 2.5V buffer models used for one [Component] would be expected to have the same min values and the same max values. Departures from this must be documented.

5.2. Model Switching Behavior Requirements

A number of parameters in the [Model] and [Model Spec] sections specify the switching characteristics of input and I/O buffers, in response to waveforms.

5.2.1. {LEVEL 3} [Model] Vinl and Vinh reasonable

The Vinl and Vinh parameters of the [Model] keyword represent the range of input threshold voltages for a population of buffers. The input threshold voltage is that voltage at which a very slowly changing input signal is able to switch the sensed input logic level from low to high or high to low. The Vinl and Vinh parameters would correspond to DC values for Vinl and Vinh in a data sheet. The [Model] Vinl and Vinh values must match corresponding values in [Model Spec], when

[Model Spec] is present. The [Model] Vinl and Vinh values are normally worst case and may correspond to typ, min, or max values in the [Model Spec] keyword, as appropriate.

For I/O buffers, Vinl and Vinh values should be below and above, respectively, Vmeas. Exceptions to this should be explained in a comment. It's uncommon.

5.2.2. {LEVEL 3} [Model Spec] Vinl and Vinh reasonable

Because the input switching uncertainty region defined by the *Vinl* and *Vinh* sub-parameters of the [Model] section (See section 5.2.2.) can be affected by power supply fluctuation for many I/O standards, a range may be specified for these parameters in the [Model Spec] section. The “min” and “max” values given must be correct for the “min” and “max” values given for the supply voltage in the [Voltage Range] keyword. Vinl and Vinh are needed only for Input and I/O types of models.

5.2.3. {LEVEL 3} [Model Spec] Vinl+/- and Vinh+/- complete and reasonable

For input buffers with different voltage thresholds for rising and falling edges, Vinh+, Vinh-, Vinl+, and Vinl- are given in the [Model Spec] section. This would be required for inputs that exhibit hysteresis, such as Schmitt trigger devices. For I/O buffers, Vinl+ and Vinh- values should be below and above, respectively, Vmeas. Exceptions to this should be explained in a comment.

5.2.4. {OPTIONAL} [Model Spec] Pulse subparameters complete

Ordinarily when an input voltage level rise above Vinl or falls below Vinh, there is a possibility that the input will switch. If the data sheet specifies that input voltage levels can rise above Vinl or fall below Vinh for short periods of time with no possibility of being sensed as an input logic level changes, then Pulse_high, Pulse_low, Pulse_time can be given in the [Model Spec] section.

While all buffers exhibit this characteristic to some degree, the IBIS format may not be flexible enough to adequately represent the behavior. Therefore a model for which this data is present in the data sheet may not have Pulse parameters in the IBIS file.

5.2.5. {LEVEL 2} [Model Spec] S_Overshoot subparameters complete and match data sheet

All input and I/O buffers have S_overshoot_high and S_overshoot_low in the [Model Spec] section. The values must match the voltage limits beyond which the device may not function correctly. These limits may be different from the absolute maximum ratings, which may be related to device destruction. The functional limits may not be found in some data sheets.

5.2.6. {LEVEL 2} [Model Spec] S_Overshoot subparameters track typ/min/max

When overshoot voltage limits are different in min and max corners, S_overshoot_high and S_overshoot_low should track these differences. For example, S_overshoot_high may increase with the higher supply voltage assumed for max mode.

5.2.7. {LEVEL 2} [Model Spec] D_Overshoot subparameters complete and match data sheet

If greater levels of overshoot can be tolerated for short periods of time, these must be given as D_overshoot_high, D_overshoot_low, and D_overshoot_time subparameters of the [Model Spec] keyword. For some technologies the data sheet may specify different parameters to address this concept. In this case the method by which D_overshoot_high, D_overshoot_low, and D_overshoot_time have been determined should be documented in the IBIS file as comments.

5.2.8. {OPTIONAL} [Model Spec] D_Overshoot subparameters track typ/min/max

When overshoot voltage limits are different in min and max corners, D_overshoot_high and D_overshoot_low should track these differences. For example, D_overshoot_high may increase with the higher supply voltage assumed for max mode.

5.2.9. {LEVEL 3} [Receiver Thresholds] Vth present and matches data sheet, if needed

If [Receiver Thresholds] are needed to represent input behavior, the Vth subparameter must be present if the signal is single-ended. Vth is the nominal input threshold voltage at voltage temperature and process conditions that define 'typ'. Vth must match the input buffer timing measurement threshold in the data sheet.

An example of a technology where [Receiver Thresholds] can be used is the DDR Memory Interface. In DDR, the input threshold voltage is nominally 0.50*VDDQ. For DDR2, VDDQ is allowed to change from 1.7 to 1.9V, nominally 1.8V. In this case Vth would be specified as 0.9V. IBIS tools will adjust the threshold voltage actually used as some system voltage fluctuates.

5.2.10. {LEVEL 3} [Receiver Thresholds] Vth_min and Vth_max present and match data sheet, if needed

Vth_min is the lowest actual input threshold voltage at typical supply voltage, process, and temperature conditions. Likewise, Vth_max is the highest actual input threshold voltage at typical supply voltage, process, and temperature conditions. These are often specified as tolerance values in data sheets, representing an uncertainty as to where Vth actually lies. Threshold changes due to min and max power supply variation are in addition to the Vth_min and Vth_max values. Vth_min and Vth_max must be present if the data sheet specifies a tolerance for Vth under typical conditions.

For example, the input threshold voltage for DDR technology is allowed to range from 0.49*VDDQ to 0.51*VDDQ, nominally 0.50*VDDQ. For DDR2, VDDQ is allowed to change from 1.7 to 1.9V, nominally 1.8V. With the above definition of Vth, Vth_min and Vth_max, the values are calculated as follows: Vth=0.9V, Vth_min=0.49*1.8=0.882V and Vth_max=0.51*1.8=0.918V. As explained above, the variation in Vth only includes the effect of change of process and temperature at nominal voltage, which in this example is 1.8V.

5.2.11. {LEVEL 3} [Receiver Thresholds] Vinh_ac, Vinl_ac present and match data sheet, if needed

Vinh_ac, Vinl_ac are the voltages above/below which the input signal must cross before the receiver can be guaranteed to change state. Vinh_ac, Vinl_ac overrides the Vinh and Vinl defined earlier in the [Model] or [Model Spec] section.

The values given for Vinl_ac and Vinh_ac must match those in the data sheet. Note, however, that these parameters are required to be specified as offsets to Vth in the IBIS model, while they may be given as absolute voltages in the data sheet. Therefore, some conversion may be necessary. For instance, taking the SSTL18 standard as an example, the data sheet might call out 0.9V for Vth and 1.150V for Vinh_ac, which would require that Vinh_ac be given the value +250 mV in the IBIS file.

5.2.12. {LEVEL 3} [Receiver Thresholds] Vinh_dc, Vinl_dc present and match data sheet, if needed

Vinh_dc and Vinl_dc are DC input voltage thresholds which determine the boundary conditions under which the receiver will NOT change state.

The values given for Vinl_dc and Vinh_dc must match those in the data sheet. Note, however, that these parameters are required to be specified as offsets to Vth in the IBIS model, while they may be given as absolute voltages in the data sheet. Therefore, some conversion may be necessary. For instance, taking the SSTL18 standard as an example, the data sheet might call out 0.9V for Vth and 1.0V for Vinh_dc, which would require that Vinh_dc be given the value +100 mV in the IBIS file.

5.2.13. {LEVEL 3} [Receiver Thresholds] Tslew_ac/Tdiffslew_ac present and match data sheet, if needed

If the data sheet specifies a maximum time that an incoming signal may take to transition between Vinl_ac and Vinh_ac, then the [Receiver Thresholds] Tslew_ac parameter should be set to that value. For differential receivers the Tdiffslew_ac parameter should be set to the maximum allowable transition time between -Vdiff_ac and +Vdiff_ac.

5.3. Model I-V Table Requirements

The term "table" as used in this document refers to rows and columns of numbers appearing in the text of the IBIS file. The term "curve" refers to the visual plotting of table data. Some checks are more easily performed visually.

The voltage columns in the [Pullup] and [Power Clamp] tables in IBIS files are Vcc-relative. This means that the voltage values in the first column are actually inverted offsets from Vcc. For example, the value at 0V in a [Pullup] table is actually measured at Vcc and the value at Vcc in the table is measured at 0V. Bear this in mind when checking Vcc-relative tables. The formula is:

```
Vtable = Vcc - Voutput
```

Curve viewing tools may offer the ability to translate Vcc-relative tables so that the curves viewed are ground relative.

5.3.1. {LEVEL 2} I-V tables have correct typ/min/max order

Inspect every I-V table. Check for proper order of the I-V tables. The order of the column values in the table must be:

VOLTAGE, Current Typ, Current Min, Current Max

In most cases the maximum current should be greater than the typical current, which should be greater than the minimum current, in the active region (e.g. where device is not clamping). The most common exception is for compensated devices, where the typical, minimum, and maximum curves may nearly overlay each other. Also, [Power Clamp] curves may exhibit crossovers due to differences in the voltages at which clamping begins.

This check is easily accomplished by viewing the curves and checking visually. Checking combined curves is preferred, but checking of individual curves is acceptable.

5.3.2. {LEVEL 2} [Pullup] voltage sweep range is correct

The voltage column in the [Pullup] table should extend from -Vcc to +2*Vcc, For the purpose of this check, Vcc is defined by the [Pullup Reference] keyword for this check, or [Voltage Range] if [Pullup Reference] is not present.

5.3.3. {LEVEL 2} [Pulldown] voltage sweep range is correct

The voltage column in the [Pulldown] table should extend from -Vcc to +2*Vcc. For the purpose of this check, Vcc is defined by the [Pullup Reference] keyword for this check, or [Voltage Range] if [Pullup Reference] is not present.

5.3.4. {LEVEL 2} [POWER Clamp] voltage sweep range is correct

The voltage column in the [POWER Clamp] should extend at least from -Vcc to 0 (it is permitted and recommended to extend from –Vcc to +2*Vcc, particularly where on-die termination is used). For the purpose of this check, Vcc is defined by the [POWER Clamp Reference] keyword for this check, or [Voltage Range] if [POWER Clamp Reference] is not present.

5.3.5. {LEVEL 2} [GND Clamp] voltage sweep range is correct

The voltage column in the [GND Clamp] should extend at least from -Vcc to +Vcc (it is permitted and recommended to extend from –Vcc to +2*Vcc, particularly where on-die termination is used). For the purpose of this check, Vcc is defined by the [POWER Clamp Reference] keyword for this check, or [Voltage Range] if [POWER Clamp Reference] is not present.

5.3.6. {LEVEL 2} I-V tables do not exhibit stair-stepping

There should be no stair stepping of any I-V tables, with flat sections and abrupt jumps. This is caused by insufficient significant digits in the table current columns. This problem appears in early versions of the NCSU s2ibis2 program. Poor measurement resolution could also cause this effect.

This check is easily accomplished by viewing the curves and checking visually.

5.3.7. {LEVEL 2} Combined I-V tables are monotonic

Check that the combined tables are monotonically increasing, ie. There are no slope reversals in the current values.

This check is easily accomplished by viewing the curves and checking visually. Alternatively, IBISCHK 4.2.1 or above will perform the same check automatically.

Note that IBISCHK reports only the first non-monotonic points in each table. After fixing the data IBISCHK should be run again.

5.3.8. {LEVEL 2} [Pulldown] I-V tables pass through zero/zero

Typ, Min, and Max [Pulldown] table currents should all pass through approximately 0 mA at the 0 volt point in the voltage column, for full swing technologies such as CMOS. All three current columns should pass through zero current at the zero volt line in the table, except in special cases (i.e. TTL, PECL, LVDS, or SERDES driver).

5.3.9. {LEVEL 2} [Pullup] I-V tables pass through zero/zero

Typ, Min, and Max [Pullup] table currents should all pass through approximately 0 mA at the 0 volt point in the voltage column, for full swing technologies such as CMOS. All three current columns should pass through zero current at the zero volt line in the table, except in special cases (i.e. TTL, PECL, LVDS, or SERDES driver).

5.3.10. {LEVEL 2} No leakage current in clamp I-V tables

For models without on-die termination, review each clamp table. The expected currents should be less than 1 uA in the normal operating ranges (typically from 0 to Vcc range in the table). IBISCHK will print a warning for clamps in which currents are never below 1uA If a table is truncated, use the extrapolated values based on the last two points prior to extrapolation. Or use a viewer which can combine the two clamp tables into one. Exceptions can exist for older TTL technologies where several milliamps may be observed and for some ECL and other technologies with which can have internal resistors. Exceptions should be understood and documented.

5.3.11. {LEVEL 2} I-V behavior not double-counted

Verify that clamping currents are found only in the [GND Clamp] and [Power Clamp] I-V tables. Verify that currents that should be found in the [Pullup] and [Pulldown] tables are not found in the [GND Clamp] and [Power Clamp] I-V tables. Verify that there is no duplication of clamping currents between the [GND Clamp] and [Power Clamp] tables. If the buffer has on-die termination, verify that termination current is not included in both the [GND Clamp] and [Power Clamp] tables in such as manner as to cause double counting of the actual current when the clamps are extrapolated and combined.

NOTE: NCSU s2ibis may not correctly model on-die termination. It places the full termination characteristic in both [Power Clamp] and [GND Clamp] tables, effectively double-counting the termination when these tables are combined by the simulator.

5.3.12. {LEVEL 2} On-die termination modeling documented

Any IBIS models with on-die termination should be labeled as such using comment lines. On die termination should be modeled in [Power Clamp] and/or [GND Clamp] tables, and possibly using [Add Submodel] if the termination is active only in non-driving mode. Document the method used to embed the termination into the clamps.

5.3.13. {LEVEL 2} ECL models I-V tables swept from -Vcc to +2*Vcc.

I-V tables in ECL models should be swept from -Vcc to +2*Vcc, where Vcc for ECL is defined as the difference between the most positive supply voltage and the most negative. This is true even though the operating range is narrower. IBIS specifies a fixed 2V range, but using the actual supply range is a better practice.

5.3.14. {LEVEL 2} Point distributions in I-V tables should be sufficient

We recommend a minimum of 10 data points at points of inflection in I-V tables to prevent interpolation issues in simulations.

5.4. Model V-T Table Requirements

5.4.1. {LEVEL 2} Output and I/O buffers have sufficient V-T tables

Push-pull Output and I/O buffers should have 2 [Rising Waveform] and 2 [Falling Waveform] tables. Open-source and Open-drain buffers may have 1 [Rising Waveform] and 1 [Falling Waveform] table. If less than 4 V-T tables are present, then this should be explained in comments.

The R_fixture value for V-T tables should be close to the characteristic impedance (Z0) of the transmission line for the application system at which the device is expected to operate. R_fixture for most legacy system is close to 50 ohm:

R_fixture connected to [Pullup Reference]

Rising V-T

Falling V-T

R_fixture connected to = [Pulldown Reference]

Rising V-T

Falling V-T

Differential and other terminated technologies may be modeled using 2 V-T tables by including a V_fixture at the common mode voltage, or close to the region of operation. For example:

R_fixture to Vcm (Common Mode Voltage)

Rising V-T

Falling V-T

For technologies such as LVDS which may not be compatible with the test fixture voltages required for [Ramp] data, at least 2 waveforms are required.

5.4.2. {LEVEL 2} V-T tables have reasonable point distribution

V-T tables should be well behaved, with continuous second derivative. V-T point density should be sufficient in areas with non-zero second derivative. For example, a low to high state transition should have at least 10 points.

This check is easily accomplished by viewing the curves and checking visually.

5.4.3. {LEVEL 3} V-T table duration is not excessive

To avoid the "over clocking" issue, excess V-T points may be removed to match the V-T duration corresponding to the maximum data rate or frequency at which the device is expected to operate. When removing trailing V-T point the final DC value must be achieved, i.e. the ending slope should be very small. Since the 2 sets of V-T tables describe the relative on and off switching delay between the pullup and pulldown transistors, relative time position between all tables with the same edge direction and corner must be maintained when removing the leading excess V-T points. The number of excess V-T points removed can be different between corners (i.e. typ, min and max) but it is recommended to explain the difference as comments of the IBIS file.

5.4.4. {LEVEL 2} V-T table endpoints match fixture voltages

If the V_fixture values equal the supply reference voltages for the [Pullup] or [Pulldown] tables, then either the starting or ending points of the V-T tables are expected to equal these V_fixture values. This applies to full swing technologies such as CMOS, and not to technologies such as TTL, PECL, LVDS, or SERDES driver, which do not necessarily swing rail to rail. This check does not apply in cases where internal pullups/pulldowns or bias conditions exist such that the combined I-V tables have current flows at the V_fixture voltages.

For example for a 3.3 V device with the [Voltage Range] set to 3.3 V, V_fixture = 3.3 V, and R_fixture = 50 ohms, the [Rising Waveform] table should end at 3.3 V, and the [Falling Waveform] table should begin at 3.3 V.

5.5. Model [Ramp] Data Requirements

The [Ramp] section is required even if [Rising Waveform] and [Falling Waveform] are present in a [Model]. [Ramp] information is used in some tools for non-simulation purposes, for example quickly finding the fastest pin on a net.

5.5.1. {LEVEL 2} [Ramp] R_load present if value other than 50 ohms

If the [Ramp] data was measured using a load resistor other than 50 ohms, the [Ramp] section has an R_load subparameter giving the load resistor value used.

5.5.2. {LEVEL 2} [Ramp] typ/min/max order is correct

The typ, min, and max [Ramp] values are taken from typ, min, and max buffer measurements. They are not necessarily sorted by dV, dt, or dV/dt. Although the progression from min to max usually has dV increasing and dt decreasing, the correct order is actually determined by the test conditions used, the same conditions used to derive typ/min/max I-V tables.

5.5.3. {LEVEL 2} [Ramp] dV consistent with I-V table calculations

The [Ramp] dV values must match values calculated by applying the [Ramp] R_load and fixture voltage values to the I-V tables for typ/min/max conditions. The high and low state voltages are determined using the I-V table calculations, and 60% of the difference between these is compared to each [Ramp] dV value. The error must not exceed 5% of the dV calculated from the I-V tables.

As of the date of this document IBISCHK does not perform this check, but future versions may. Current IBISCHK versions can be used to perform this check by making temporary modifications to the IBIS [Model], adding [Rising Waveform] and [Falling Waveform] keywords with V_fixture and R_fixture values corresponding to the correct [Ramp] fixture values, as described in IBIS Specification section 9 (Notes of Data Derivation Method), item 3 (Ramp Rates). These waveforms would have 2 points giving artifical initial and final voltage values, chosen to force IBISCHK to declare an error and report calculated values. These values calculated by IBISCHK can be used to calculate the 20% to 80% dV for comparison to [Ramp] dV.

5.5.4. {LEVEL 2} [Ramp] dt is consistent with 20%-80% crossing time

Each dt value matches within 10% the difference between the times of crossing the 20% voltage point and the 80% voltage point on the corresponding [Rising Waveform] or [Falling Waveform] with test fixture most similar to the [Ramp] test fixture, if matching V-T tables are present

This check is to be performed using V-T tables with V_fixture or R_fixture matching [Ramp] fixture values. The waveform R_fixture must match [Ramp] R_load, or 50 ohms if not specified. The [Rising Waveform] must have V_fixture equal to 0V. The [Falling Waveform] must have V_fixture, V_fixture_min, and V_fixture_max values must correspond to the [Pullup Reference] or [Voltage Range] typ, min, and max values, respectively. Reasonably small values of C_fixture, L_fixture, R_dut, L_dut, and C_dut parameters in [Rising Waveform] and [Falling Wavform] can be overlooked in the V-T table selection process, although these may degrade the correlation of [Ramp] to V-T table endpoints.

If suitable waveforms for this check are not present, an appropriate alternate reference for dt may be chosen. This may be simulated or measured waveforms, or a datasheet.

5.6. Output timing checks

5.6.1. {LEVEL 3} [Model Spec] Vmeas and Vref used if typ/min/max variation

Usually Vref and Vmeas have the same value for push-pull technologies, and are specified to vary in proportion to supply voltage for typ/min/max conditions. Vmeas and Vref parameters in a [Model Spec] keyword would be used to convey any typ/min/max variation of these.

5.6.2. {LEVEL 3} Vref consistent for Open-drain, Open-source, and ECL Model_types

For Open-drain models [Model] or [Model Spec] Vref must be above Vmeas, and it is usually set to the [Pullup Reference] voltage. For Open-source and Open-sink models Vref must be below Vmeas, and it is usually set to the [Pulldown Reference] voltage, typically zero. For ECL models Vref must be below Vmeas, and is usually 2V below [Pullup Reference].

6. Correlation

IBIS quality correlation designator "S" specifies that the model developer has simulated a buffer using identical test loads in SPICE and in IBIS, and compared the results. Likewise, the “M” designator specifies that IBIS simulations and bench measurements have been compared. The intention of correlation is to assess the degree to which the IBIS model data will result in

simulations that match SPICE simulations and/or bench measurements. By careful attention to detail and understanding the behavior of the I/O circuit, it is possible to achieve extremely close correlation between SPICE and IBIS simulation results. Be aware that not all IBIS behavioral simulators are created equal; discrepancies may be an artifact of the behavioral simulator rather than the IBIS model extraction process.

If the “M” and/or “S” correlation designators are used the methods employed and results must be thoroughly documented. If the documentation is external to the IBIS file, the IBIS file must contain comments sufficient to locate the correlation documentation. Inclusion of golden waveforms, either in external documents or in the IBIS file as [Test Data]/[Test Load] sections, or both, is recommended.

For detailed information please refer to the "I/O Buffer Accuracy Handbook":

http://www.eda.org/pub/ibis/accuracy/

The I/O Buffer Accuracy Handbook defines quantitative methods for correlating hardware measurements, SPICE simulations and IBIS simulations, and documenting the results of the correlation. It describes general principles such as overlay and envelope metrics, test circuits, and specific figures of merit to grade correlation results. Correlation methods are not limited to those described in the I/O Buffer Accuracy Handbook, but all methods used must be documented if the “M” and/or “S” designators are used.